OpenVPX™ Trends and Updates

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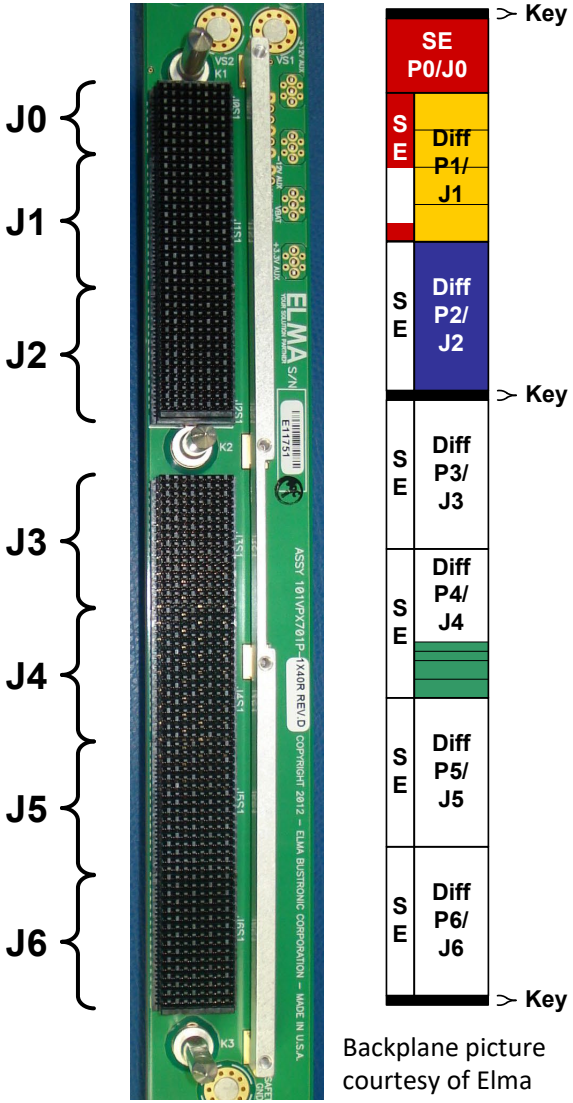
Outline

- **OpenVPX and associated standards**
- **Relationship of OpenVPX with other standardization efforts**
- **OpenVPX plans and trends**
  - Connecter Modules in ANSI/VITA 65.1-2017, 2019, 2021, and expected 2023
  - Alternative Module Profile Scheme (AMPS)
  - Slot and Backplane Profiles added with 65.0-2019, 2021, and expected 2023
  - Protocol sections added with ANSI/VITA 65.0-2019, 2021, and expected 2023
- **Summary**



Backplane picture courtesy of Elma

Some of these slides were taken from the OpenVPX Tutorial. The full Tutorial as well as some others is available at: http://www.vita.com/Tutorials

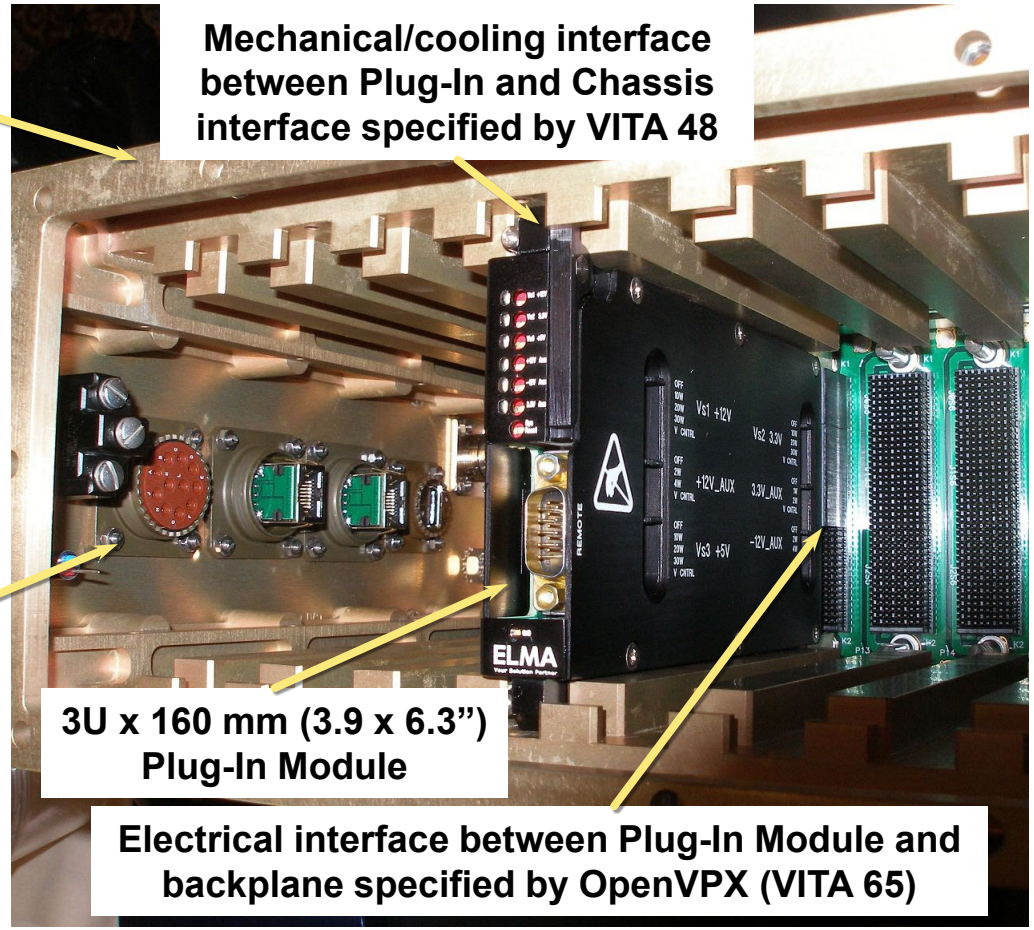
OpenVPX and Associated Standards

Conduction cooled chassis

Channels for cooling air

Chassis front panel

Pictures courtesy of Elma



Mechanical/cooling interface between Plug-In and Chassis interface specified by VITA 48

3U x 160 mm (3.9 x 6.3”) Plug-In Module

Electrical interface between Plug-In Module and backplane specified by OpenVPX (VITA 65)

- These standards define interfaces between Plug-In Modules and chassis for products intended to be deployed in harsh environments

Relationship of OpenVPX to Other Standardization Efforts

- **For what goes into OpenVPX, continuing to get input from:**
  - VITA Member companies
  - SOSA (Sensor Open Systems Architecture) Hardware Working Group (https://www.opengroup.org/sosa)
  - HOST (Hardware Open Systems Technologies) community of both those working on it and those using it (https://host-oa.com/)
  - Army C5ISR Center's CMOSS (C4ISR/EW Modular Open Suite of Standards) Community thru their influence of SOSA
- **Also taking input from VITA 65 Working Group back to SOSA**
  - Several of us participate in both VITA and SOSA
- **In SOSA we have discussions, which are ITAR controlled, to come up with best solutions in relation to target applications**
  - The VITA Standards Organization (https://www.vita.com/) is international, so we cannot have discussions involving ITAR controlled and other sensitive information
- **Working to align SOSA, HOST, CMOSS and OpenVPX**
  - In terms of Slot and Module Profiles, expect SOSA, HOST, and CMOSS to continue to point at a subset of OpenVPX

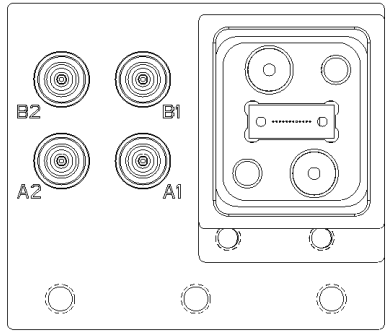
OpenVPX Plans and Trends (1 of 2)

- **Latest versions of OpenVPX™ Published October 2021**
  - **ANSI/VITA 65.0-2021, OpenVPX™ System Standard; October 2021**
  - **ANSI/VITA 65.1-2021, OpenVPX™ System Standard – Profile Tables; October 2021**
- **ANSI/VITA 65.0-2021 and ANSI/VITA 65.1-2021 added:**
  - **16 Connector Modules to VITA 65.1, in addition to the 10 that are in ANSI/VITA 65.1-2019**
  - **AMPS (Alternate Module Profile Scheme) – use of string to specify Module Profile**
    - Enumeration of lots more optical/coax options in combination with protocol options became impractical
    - Classic Module Profiles allow ports to not be implemented as long as it does not implement a different protocol
  - **Ethernet, Aurora, General Purpose Serial, and General Purpose Electrical protocol sections**
  - **Only 1 new 6U Slot Profile and 2 new 6U Backplane Profiles**
    - Compared to 5 new 6U and 6 new 3U Slot Profiles added with ANSI/VITA 65.0-2019
  - **Enable use of higher speed VPX connectors:**
    - ANSI/VITA 46.30-2020, Higher Data Rate VPX; July 14, 2020
    - VITA 46.31-2020-VDSTU, Higher Data Rate VPX, Solder Tail; Rev 1.61, September 10, 2020

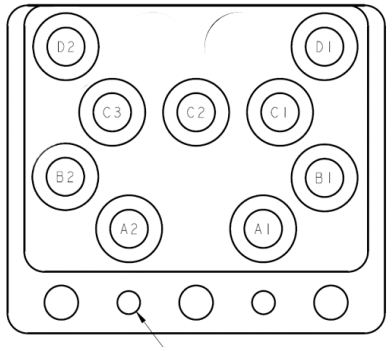
OpenVPX Plans and Trends (2 of 2)

- **Working on next versions of VITA 65.0 & 65.1, expect out early 2023, expected to add:**
  - **2 Connector Modules to VITA 65.1 – these add 75 ohm contacts for video**
  - **Protocol sections**
    - Additional of Ethernet protocols at 26.5625 Gbaud using PAM4 – 50 Gbits/s per lane
    - Addition of sFPDP (Serial Front Panel Data Port) – ANSI/VITA 17.1-1997 (S2021) and ANSI/VITA 17.3-2018
    - Addition of a few more General Purpose electrical
    - Addition of Video protocols
  - **No new Slot or Backplane Profiles other than Slot Profile dash options**
    - Slot Profiles dash options (are in VITA 65.1) specify what Connector Modules go in apertures for optical/coax
    - Slot Profile dash options also specify Optical Profiles – how pipes for protocols are mapped to MTs
    - Regardless of the Slot Profile dash option, the aperture (hole) in the backplane stays the same
- **With version after 2023**
  - **Expect new protocol sections, maybe some new Slot Profiles, Slot Profile dash options, . . .**
- **Working out what next generation VPX connectors are and how to standardize them**

Connector Modules In ANSI/VITA 65.1-2017

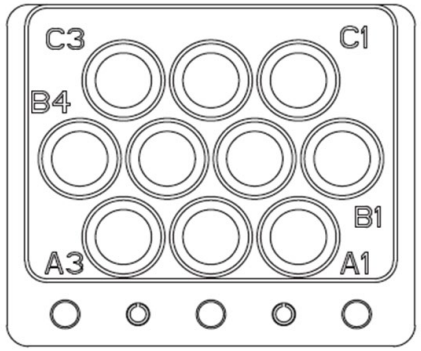


Hybrid_66.4+67.1-6.4.5.6.1



9_SMPM_contacts-6.4.5.6.2

- **ANSI/VITA 65-2010 (R2012) has only two Slot Profiles with optical/coax**
  - These Slot Profiles have ANSI/VITA 67.1 Connector Modules – 4 RF contacts
  - No optical
- **ANSI/VITA 65.1-2017 was the initial version of 65.1**
  - ANSI/VITA 65-2010 and 65-2010 (R2012) have tables of Module and Backplane Profile dash options included – these moved to VITA 65.1
  - ANSI/VITA 65-2010 and 65-2010 (R2012) do not have Slot Profile dash options – added with VITA 65.1
  - OpenVPX Connector Module definitions are in VITA 65.1



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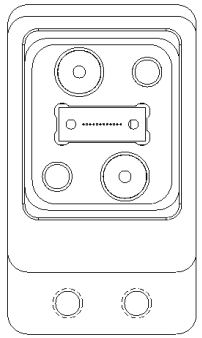
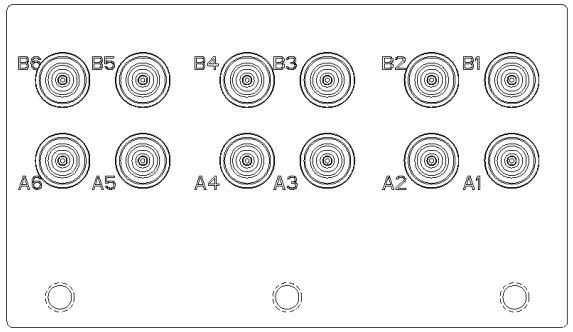
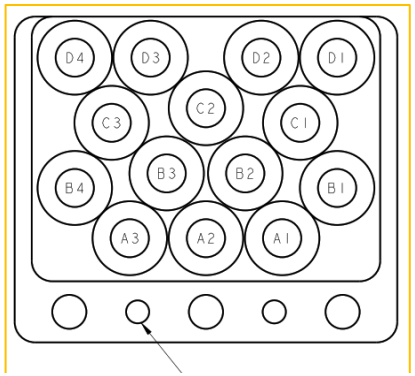


66.4_in_67.3D-6.4.5.7.1



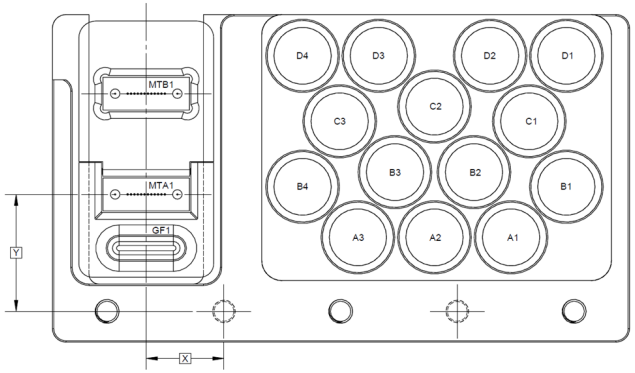
3_of_67.1_in_67.3E-6.4.5.8.1

Connector Modules Added by ANSI/VITA 65.1-2019



14_SMPM_contacts-6.4.5.6.4

- **With what is expected to be 2023 version of 65.1 all Connector Modules using ANSI/VITA 66.5-2022 Style B are not recommended for new designs**
  - Style B has been superseded by Style D
  - Style B is included in ANSI/VITA 66.5-2022 to document existing designs
  - ANSI/VITA 65.1-2019 and 65.1-2021 do not include Recommendation to not use Style B in new designs



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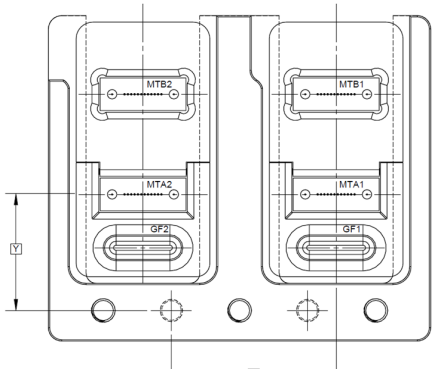
(not recommended for new designs)



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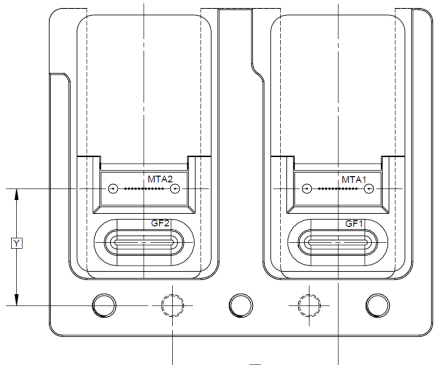

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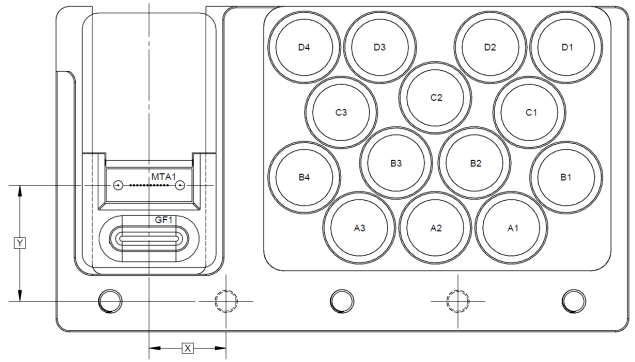

1_Style_C_66.5_insert_and_
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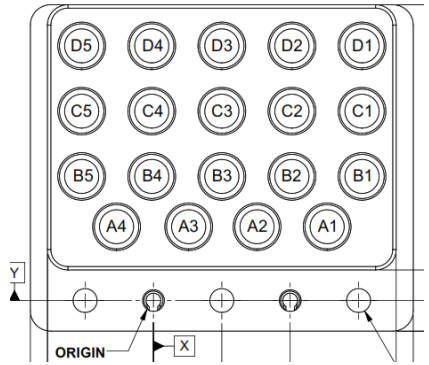
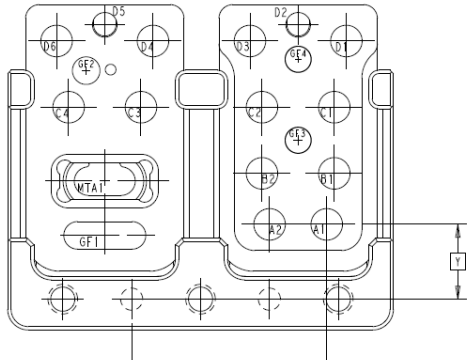
Connector Modules Added by ANSI/VITA 65.1-2021 (1 of 3)

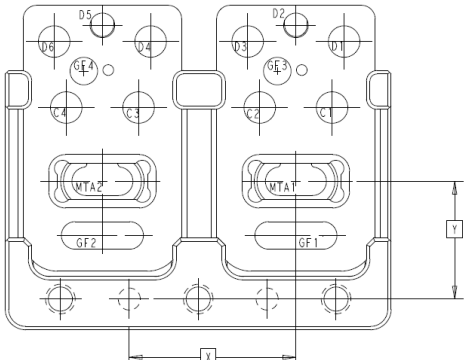


19_SMPS_contacts-6.4.5.6.7



1_Style_C_insert_and_
14_NanoRF_contacts-6.4.5.6.9

- **Addition of Connector Modules peaked with ANSI/VITA 65.1-2021**
  - There are 5 in ANSI/VITA 65.1-2017
  - 5 added with ANSI/VITA 65.1-2019
  - 16 added with ANSI/VITA 65.1-2021
  - 2 with what is expected to be 2023 version



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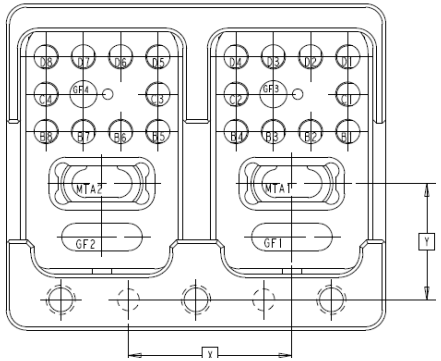

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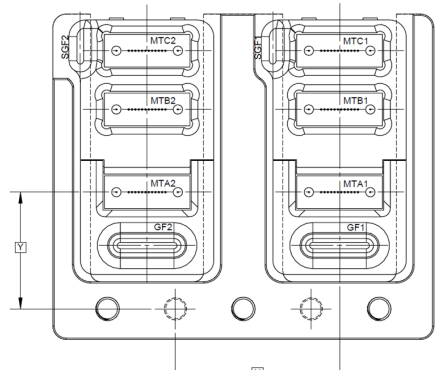

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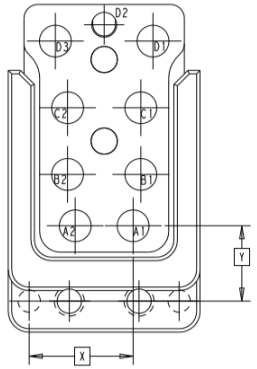
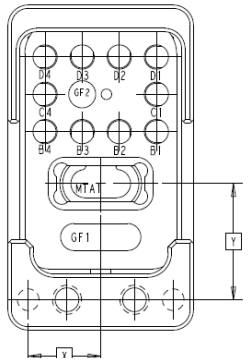
Connector Modules Added by ANSI/VITA 65.1-2021 (2 of 3)



9_NanoRF_contacts-6.4.5.7.2



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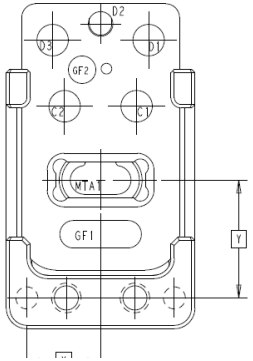

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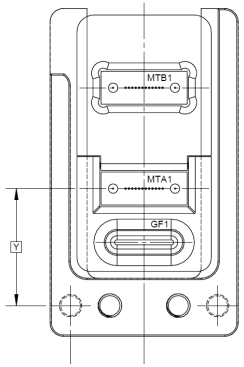

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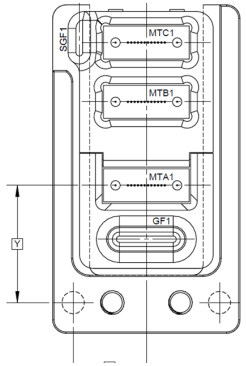
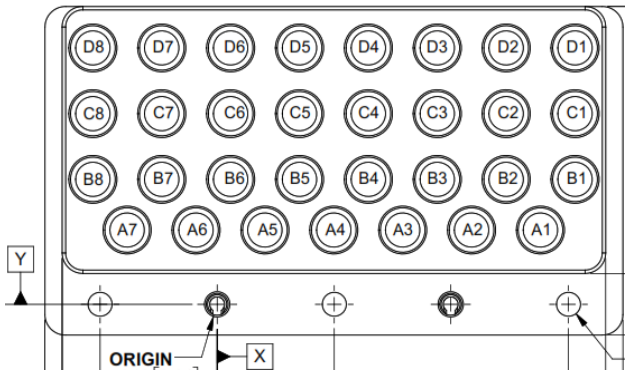
(not recommended for new designs)

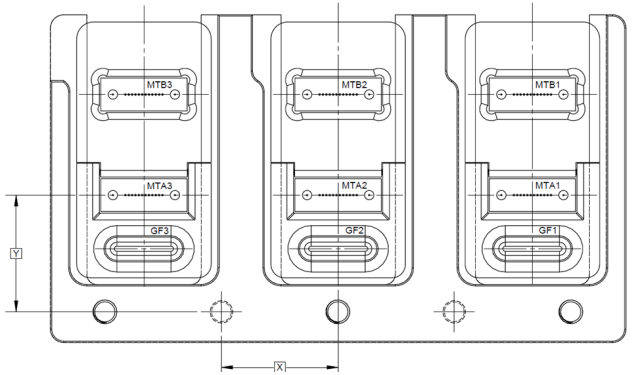


1_Style_D_insert-6.4.5.7.6

Connector Modules Added by ANSI/VITA 65.1-2021 (3 of 3)



31_SMPS_contacts-6.4.5.8.4



3_Style_B_inserts-6.4.5.8.6
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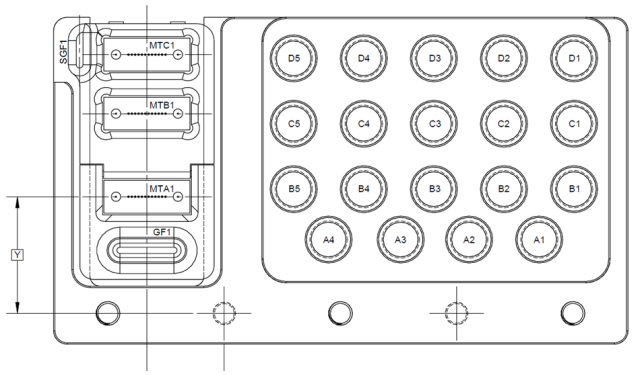
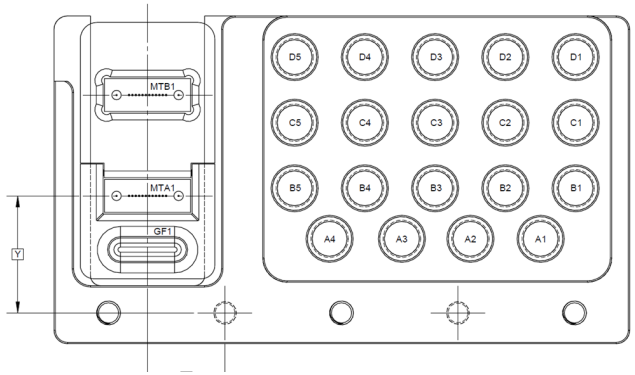
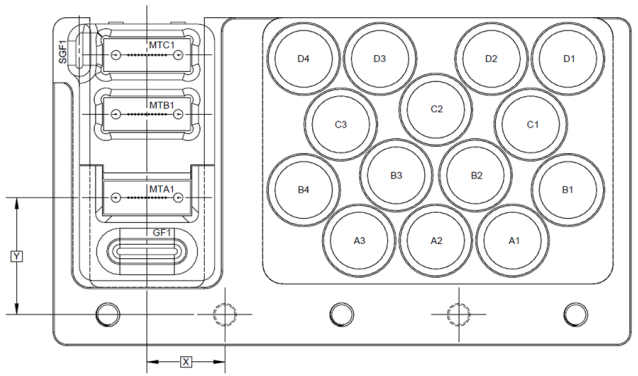


1_Style_D_insert_and_
19_SMPS_contacts-6.4.5.8.8



1_Style_B_insert_and_19_SMPS_contacts-6.4.5.8.5
(not recommended for new designs)



1_Style_D_insert_and_
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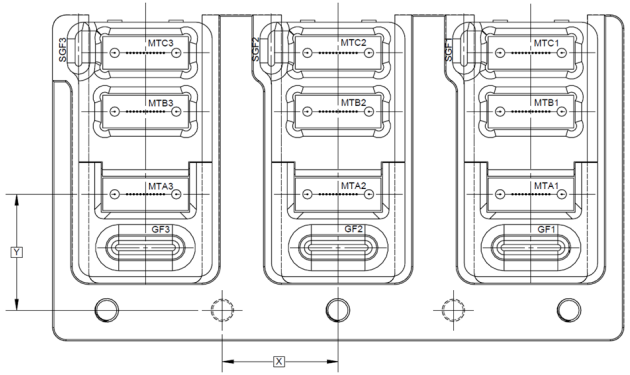
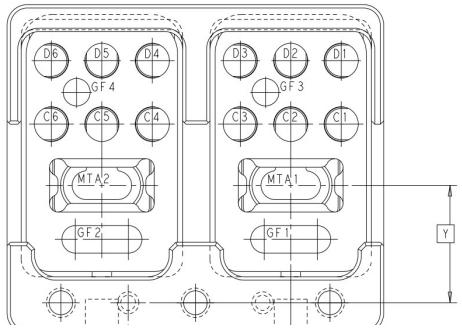


3_Style_D_inserts-6.4.5.8.9

Connector Modules Added by Version of VITA 65.1 Expected In 2023



2_Style_C_inserts_and_
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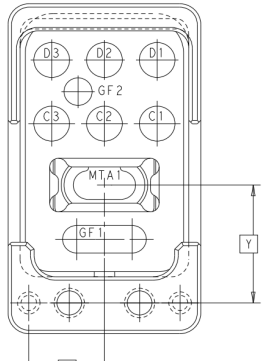
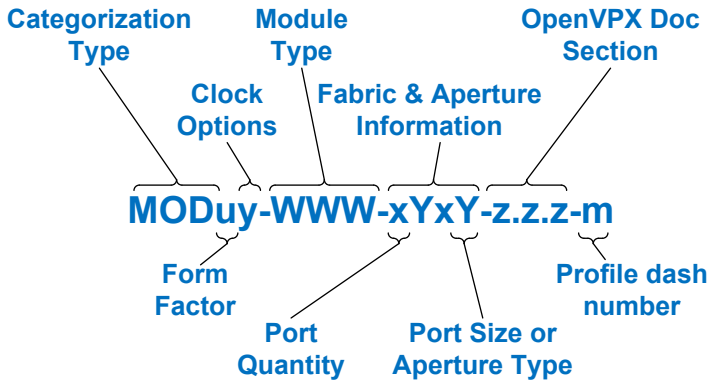


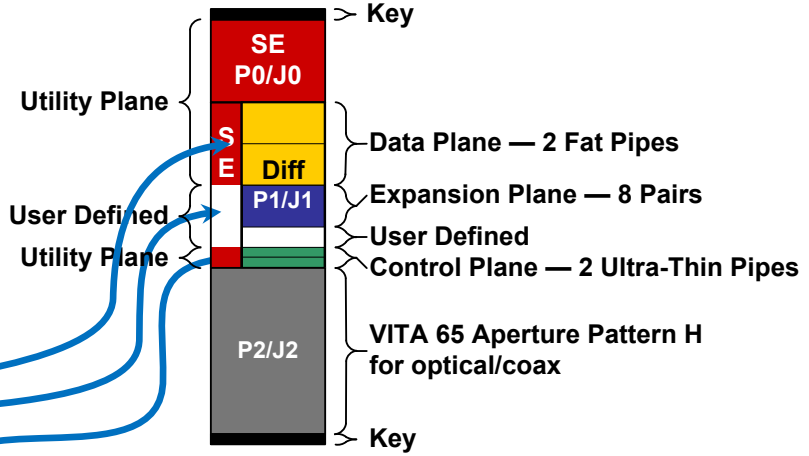
1_Style_C_insert_and_
6_75-OhmNanoRF contacts-6.4.5.7.7

- **Adds Connector Modules with 75 ohm contacts**
  - Intended to be used with video protocols

[VITA 65.1] Excerpt – Classic Module Profiles

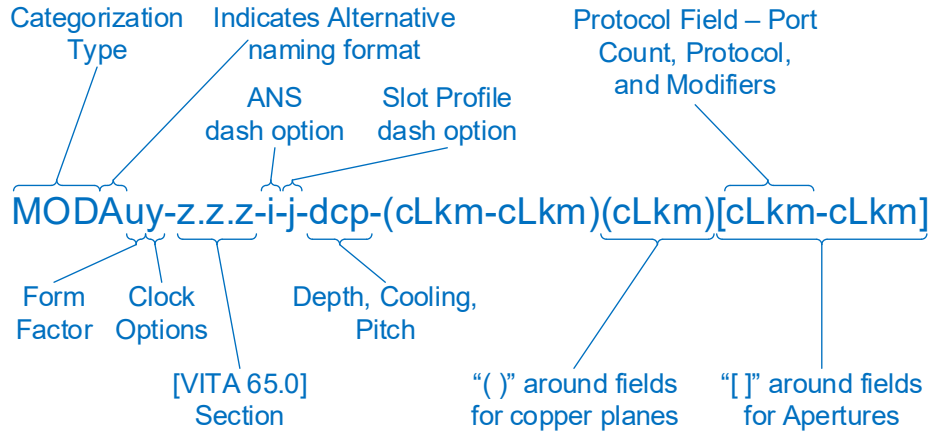


- **[VITA 65.1] excerpt for MOD6-PAY-4F1Q2U2T-12.2.1-n given at bottom**
- **Module Profiles specify a particular Slot Profile and the protocols that go on groups of pins**
  - Slot Profile dash options specify which optical/coax Connector Modules are present
- **Slot Profile diagram given middle right**
- **Module Profile name construction given in upper right**
  - Same as Slot Profile name construction except for “MOD” vs “SLT”
  - The section number and dash number at the end of the name make sure it is unique
- **Dash number used to specify a particular combination of protocols and the Slot Profile**
  - For a given Module Profile, only the dash number of the Slot Profile varies
- **With the addition lots of optical/coax options, enumerating all the desired combinations became unwieldy**



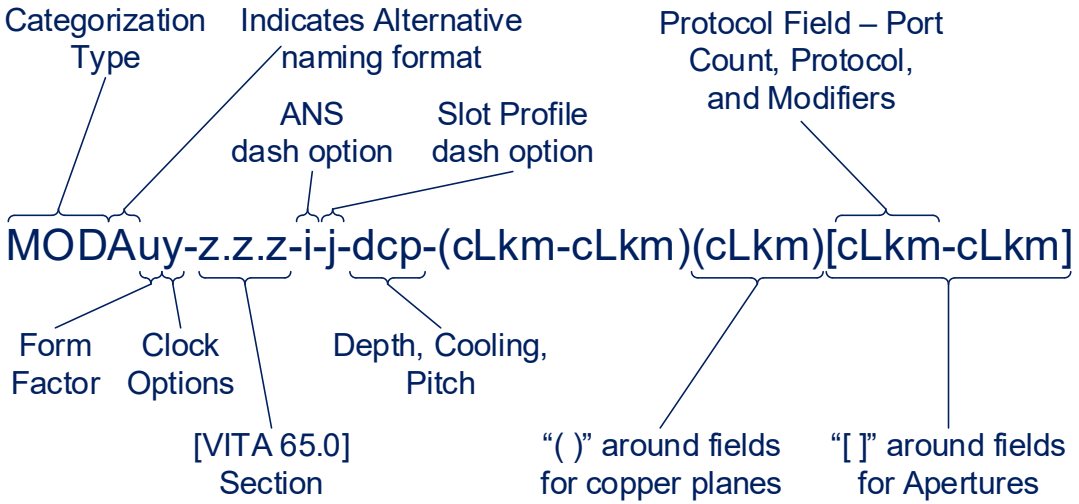
Module Profile names	Dash Num	STD Date	Slot Profile	Protocols for Copper Planes: Data Plane	Expansion Plane	Control Plane	Protocols for Optical	Comments
MOD3-PAY-2F1F2U1H-16.6.3-				**DP01, DP02**	**EP00 - EP03**	**CPutp01, CPutp02**		**First row of MOD3-PAY-2F1F2U1H-16.6.3-n**
MOD3-PAY-2F1F2U1H-16.6.3-	1	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-0	PCIe Gen 3 -- 5.3.3.3	User Defined	1000BASE-KX -- 5.1.2		
MOD3-PAY-2F1F2U1H-16.6.3-	2	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-0	10GBASE-KR -- 5.1.8	User Defined	1000BASE-KX -- 5.1.2		
MOD3-PAY-2F1F2U1H-16.6.3-	3	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-0	40GBASE-KR4 -- 5.1.8	User Defined	1000BASE-KX -- 5.1.2		
MOD3-PAY-2F1F2U1H-16.6.3-	4	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-1	PCIe Gen 3 -- 5.3.3.3	PCIe Gen 3 -- 5.3.3.3	1000BASE-KX -- 5.1.2		P2 has 9 of SMPM contacts
MOD3-PAY-2F1F2U1H-16.6.3-	5	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-1	10GBASE-KR -- 5.1.8	10GBASE-KR -- 5.1.8	1000BASE-KX -- 5.1.2		P2 has 9 of SMPM contacts
MOD3-PAY-2F1F2U1H-16.6.3-	6	2017-05	SLT3-PAY-2F1F2U1H-14.6.3-1	PCIe Gen 3 -- 5.3.3.3	10GBASE-KR -- 5.1.8	1000BASE-KX -- 5.1.2		P2 has 9 of SMPM contacts
Last line								

Alternate Module Profile Scheme (AMPS)



- **Instead of a list of fixed Module Profile dash options; use a string with a field specifying protocol for each port – referred to as an AMPS String**
  - A Plug-In Module product specification can indicate, in the AMPS String, the implementation of all ports
- **All protocols listed required to be implemented, except where AMPS String indicates port is dormant**
  - With classic Module Profiles it is legal to not implement some ports/lanes
    - For more on this, in [VITA 65.0] see Sections:
      - 6.2.2 Which lanes, Ports and Pins are Used (Unused = Reserved) & 8.4 Unused Ports, Lanes, and Utility Plane Signals
  - For ports with some lanes not implemented have a modifier for the field which specifies which lanes are present
- **Ports configurable for multiple protocols implement all the lanes with the configured protocol**
  - For example if an FP is configured to 10GBASE-KR, then it must be repartitioned into 4 UTPs all with 10GBASE-KR
- **To have a string indicate all the protocols on all the ports of a Plug-In Module; need following:**
  - A mapping for the possible values of a field in the string to protocols – Protocol Fields
  - A method for defining which Protocol Field in the string goes with which port of the Plug-In Module – an ANS (Alternate Naming Structure)

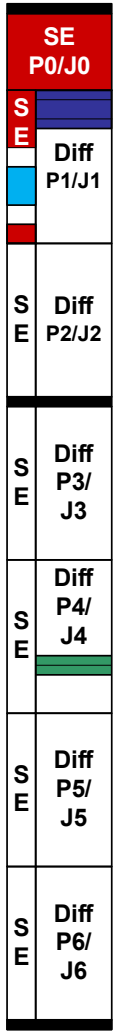
AMPS String Examples



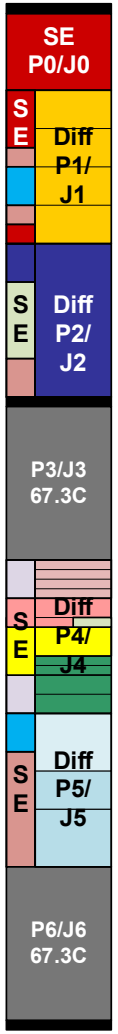
- **Upper part of table gives Classic Module Profile dash options; bottom gives Alternate Naming Structure for AMPS**
- **In these examples assume for dcp assume 160 mm depth, 1.0 inch pitch and [VITA 48.2] cooling = F2C**
- **Equivalent Module Profiles expressed with Classic Module Profile Name construct and AMPS**
  - Classic: MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-11
    AMPS: **MODA3p-16.6.11-1-4-F2C-(E8-E7)(P3F-P3F)(E7)(N-G5)**
  - Classic: MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-12
    AMPS: **MODA3p-16.6.11-1-4-F2C-(E8-E7)(P3F-G2)(E7)(N-G5)**

Module Profile names	Dash Num	STD Date	Slot Profile	Protocols for Copper Planes					Miscellaneous Protocols over copper connectors		Protocols for Optical/Coax
				Data Plane	Data Plane	Expansion Plane	Expansion Plane	Control Plane			
MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-				**DP01**	**DPutp01**	**EP00 - EP03**	**EP04 - EP07**	**CPutp01**	**GPIO1**	**CLK1orGP**	**Protocols for Optical/Coax**
MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-	1	2017-05	SLT3p-PAY-1F1U1S1S1U1U2F1H-14.6.11-1	10GBASE-KX4 -- 5.1.5	1000BASE-KX -- 5.1.2	PCIe Gen 2 -- 5.3.3.2	User Defined	1000BASE-KX -- 5.1.2	Reserved	CLK -- 5.15.5	
MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-	2	2019-11	SLT3p-PAY-1F1U1S1S1U1U2F1H-14.6.11-2	10GBASE-KX4 -- 5.1.5	1000BASE-KX -- 5.1.2	PCIe Gen 2 -- 5.3.3.2	User Defined	1000BASE-KX -- 5.1.2	Reserved	CLK -- 5.15.5	
• • •											
MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-	11	2019-11	SLT3p-PAY-1F1U1S1S1U1U2F1H-14.6.11-4	40GBASE-KR4 -- 5.1.8	10GBASE-KR -- 5.1.7	PCIe Gen 3 -- 5.3.3.3	PCIe Gen 3 -- 5.3.3.3	10GBASE-KR -- 5.1.7	Reserved	CLK -- 5.15.5	
MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-	12	2019-11	SLT3p-PAY-1F1U1S1S1U1U2F1H-14.6.11-4	40GBASE-KR4 -- 5.1.8	10GBASE-KR -- 5.1.7	PCIe Gen 3 -- 5.3.3.3	GPLVDS -- 5.15.2	10GBASE-KR -- 5.1.7	Reserved	CLK -- 5.15.5	
• • •											
MODA3-16.6.11-		**STD Date**	**Slot Profile**	**Protocols for Copper Planes**					**Miscellaneous Protocols over copper connectors**		**Protocols for Optical/Coax**
MODA3-16.6.11-	1	2021-10	SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n	(DP01	DPutp01)	(EP00 - EP03	EP04 - EP07)	(CPutp01)	(GPIO1	CLK1orGP)	[P2]
Last line											

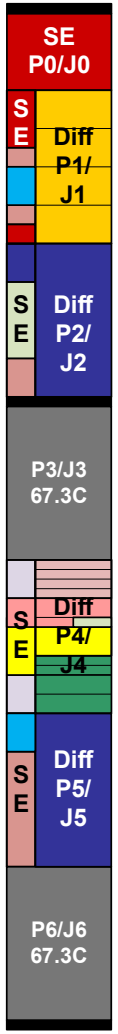
6U Slot Profiles Added by ANSI/VITA 65.0-2019



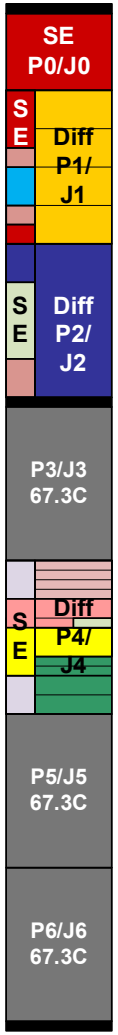
SLT6-PAY-4U2U-10.2.8



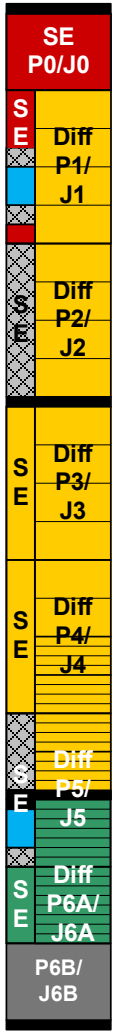
SLT6-PAY-. . .-10.6.3-n



SLT6-PAY-. . .-10.6.4-n



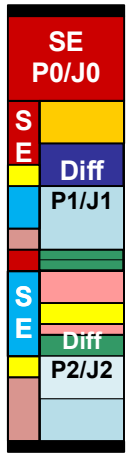
SLT6-PAY-. . .-10.6.5-n



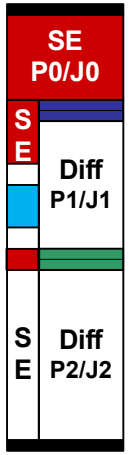
SLT6-SWH-. . .-10.8.1

- **Module Profiles for these Slot Profiles only use the following for power from the backplane:**
  - 12 VDC (VS1 and VS2)
  - 3.3V_AUX
  - VBAT
- **SLT6-PAY-4U2U-10.2.8 is the only one of these with UD (User Defined) pins**
- **No new Backplane Profiles added with ANSI/VITA 65.0-2019**

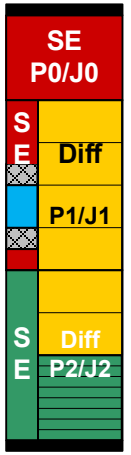
3U Slot Profiles Added by ANSI/VITA 65.0-2019



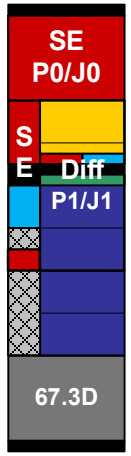
SLT3-PAY-. . .-14.2.16



SLT3-PAY-2U2U-14.2.17

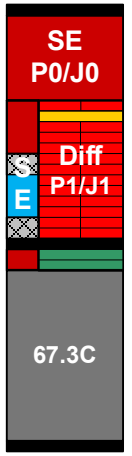


SLT3-SWH-6F8U-14.4.15



SLT3-PAY-. . .-14.6.13

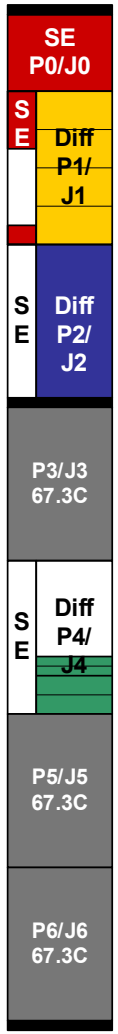
SLT3-PAY-. . .-14.6.14



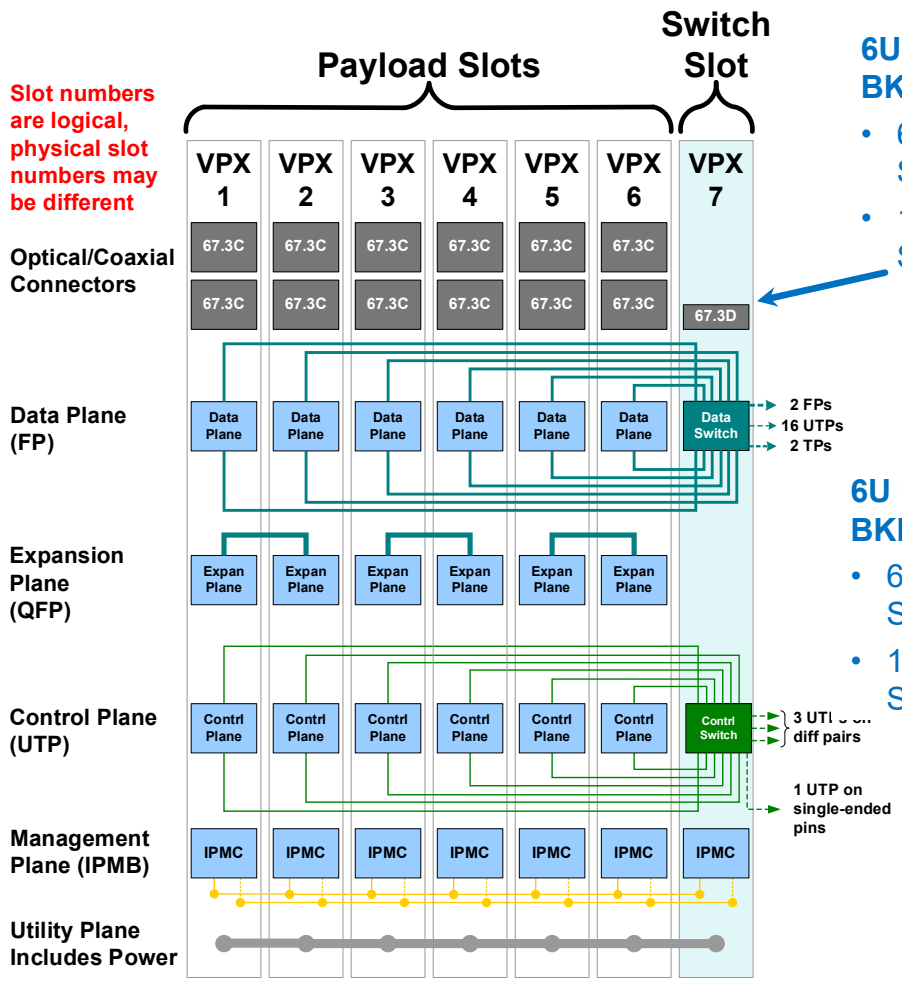
SLT3-PAY-. . .-14.9.2

- **Module Profiles for these Slot Profiles only use the following for power from the backplane:**
  - 12 VDC (VS1)
  - 3.3V_AUX
  - VBAT
- **SLT3-PAY-2U2U-14.2.17 is the only one of these with UD (User Defined) pins**

Slot Profiles and Backplane Profiles Added with ANSI/VITA 65.0-2021



SLT6-PAY-. . .-10.6.6

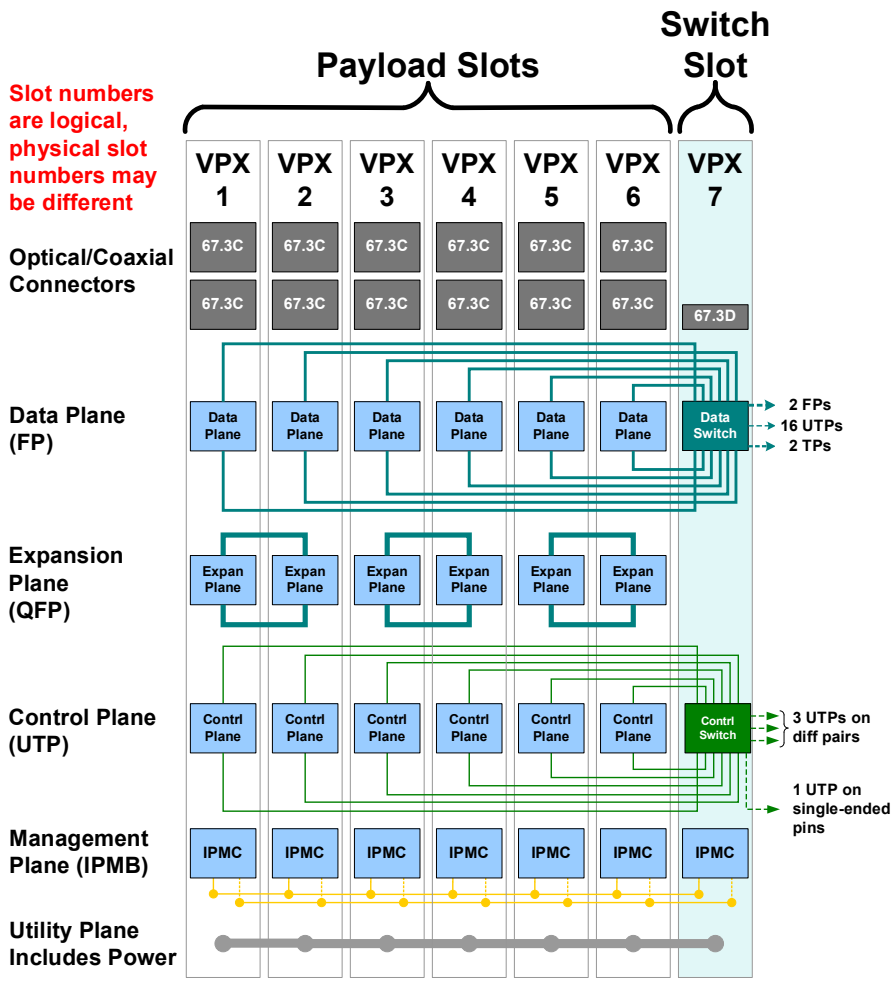


6U Backplane Profile BKP6-CEN07-11.3.3-n

- 6 Payload: SLT6-PAY-. . .-10.6.3-n
- 1 Switch: SLT6-SWH-. . .-10.8.1

6U Backplane Profile BKP6-CEN07-11.3.4-n

- 6 Payload: SLT6-PAY-. . .-10.6.4-n
- 1 Switch: SLT6-SWH-. . .-10.8.1



- **One new Slot Profile and 2 Backplane Profiles were only ones added other than dash options**
  - With what is expected to be the 2023 versions of VITA 65.0 and 65.1 there are no new profiles other than dash options

Protocol Sections Added With ANSI/VITA 65.0-2019 (1 of 2)

- **Ethernet sections added**
  - **5.1.14** 100BASE-TX (0.125 Gbaud Signaling)
  - **5.1.15** 25GBASE-KR (25.78125 Gbaud Signaling)
  - **5.1.16** 25GBASE-KR-S (25.78125 Gbaud Signaling)
  - **5.1.17** 25GBASE-SR (25.78125 Gbaud Signaling Over Multimode Optical Fiber)
  - **5.1.18** 100GBASE-KR4 (25.78125 Gbaud Signaling)
  - **5.1.19** 100GBASE-SR4 (25.78125 Gbaud Signaling Over Multimode Optical Fiber)
- **InfiniBand section added**
  - **5.4.6** InfiniBand EDR (25.78125 Gbaud Signaling)

Protocol Sections Added With ANSI/VITA 65.0-2019 (2 of 2)

- **5.9 USB (Universal Serial Bus)**
  - **5.9.1** High-Speed USB 2 (0.480 Gbaud Signaling)
  - **5.9.2** SuperSpeed USB 3 Gen 1 (5 Gbaud Signaling)
  - **5.9.3** SuperSpeed USB 3 Gen 2 (10 Gbaud Signaling)
- **5.13 General purpose serial ports**
  - **5.13.1** Asynchronous Serial Ports [TIA-422] and [TIA-232] (at least up to 115,200 baud)
  - **5.13.2** Asynchronous Serial Ports with LVCMOS Levels (at least up to 115,200 baud)
- **5.14 Signals Over Coax**
  - **5.14.1** Digital Over coax – Analog Levels
  - **5.14.2** Digital Over coax – CMOS/TTL levels
  - **5.14.3** GPS Antenna Input
- **5.15 General purpose electrical**
  - **5.15.1** GPIO – Single-Ended General Purpose I/O
  - **5.15.2** GPLVDS – Differential General Purpose I/O

Protocol Sections Added With ANSI/VITA 65.0-2021

- **Ethernet sections added**
  - **5.1.20** 50GBASE-KR2 (25.78125 Gbaud Signaling)
  - **5.1.21** 50GBASE-SR2 (25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **Aurora sections added**
  - **5.7.3** Aurora with 64B/66B Encoding (up to 10.3125 Gbaud Signaling)
  - **5.7.4** Aurora with 64B/66B Encoding (up to 25.78125 Gbaud Signaling)
  - **5.7.5** Aurora with 64B/66B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
  - **5.7.6** Aurora with 64B/66B Encoding (up to 25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **General purpose serial port sections added**
  - **5.13.3** Asynchronous Serial Ports [TIA-232]
  - **5.13.4** Asynchronous Serial Ports [TIA-422]
  - **5.13.5** Asynchronous Serial Ports [TIA-485]
- **General purpose electrical sections added**
  - **5.15.3** [TIA-485] Higher-voltage, Differential, Bi-Directional General Purpose I/O
  - **5.15.4** [TIA-422] Higher-voltage, lower-speed Differential General Purpose I/O
  - **5.15.5** CLK – Electrical requirements of radial clocks

Non-Video Protocol Sections Expected to be Added in 2023

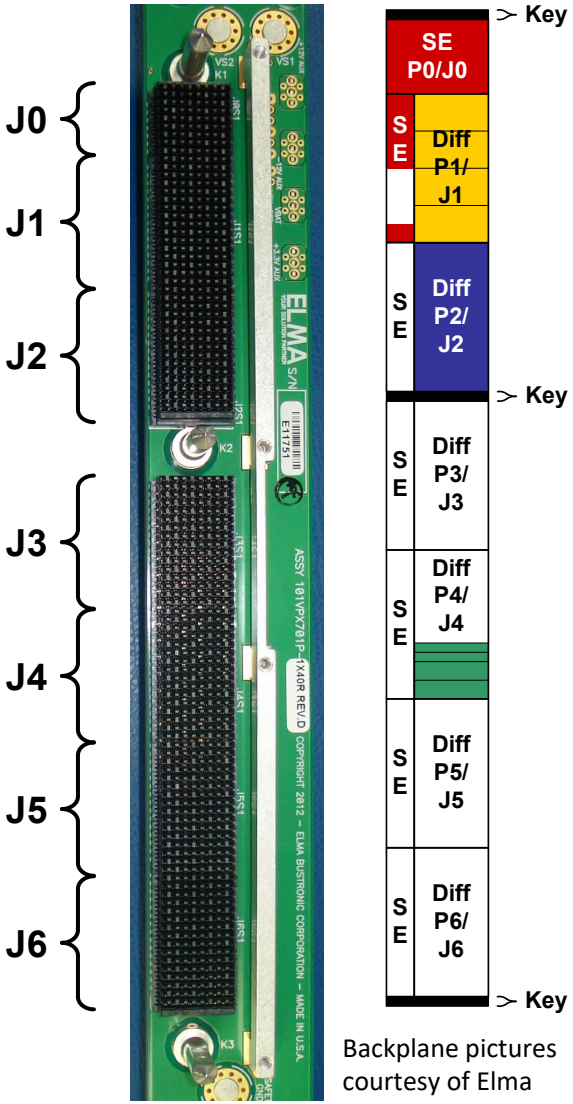
- **Ethernet sections added**
  - **5.1.22** 50GBASE-KR – (26.5625 Gbaud, PAM4 Signaling)
  - **5.1.23** 100GBASE-KR2 – (26.5625 Gbaud, PAM4 Signaling)
  - **5.1.24** 200GBASE-KR4 – (26.5625 Gbaud, PAM4 Signaling)
  - **5.1.25** 400GBASE-KR8 – (26.5625 Gbaud, PAM4 Signaling)
- **5.16 Serial Front Panel Data Port (sFPDP)**
  - **5.16.1** sFPDP with 8B/10B Encoding (up to 10.3125 Gbaud Signaling)
  - **5.16.2** sFPDP with 8B/10B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
  - **5.16.3** sFPDP with 64B/67B Encoding (up to 10.3125 Gbaud Signaling)
  - **5.16.4** sFPDP with 64B/67B Encoding (up to 25.78125 Gbaud Signaling)
  - **5.16.5** sFPDP with 64B/67B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
  - **5.16.6** sFPDP with 64B/67B Encoding (up to 25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **General purpose electrical sections added**
  - **5.15.6** LVGPIO – Single-Ended General Purpose I/O
  - **5.15.7** GPLVDS15 – Differential General Purpose I/O Using 1.5V Logic

Video Protocol Sections Expected to be Added in 2023

- **5.17 Composite Video Baseband Signal (CVBS)**
  - **5.17.1** National Television System Committee (NTSC)
- **5.18 Analog Video for Aircraft System**
  - **5.18.1** STANAG 3350 Class A – 875 lines, 60 Hz field frequency
  - **5.18.2** STANAG 3350 Class B – 625 lines, 50 Hz field frequency
  - **5.18.2** STANAG 3350 Class C – 525 lines, 60 Hz field frequency
- **5.19 Video Signal/Data Serial Interface (SDI)**
  - **5.19.1** High-Definition Serial Digital Interface (HD-SDI) & **5.19.2** 3 Gbit/s Serial Data Interface (3G-SDI)
- **5.20 CoaXPress**
  - **5.20.1** CoaXPress CXP-1 – 1.250 Gbits/s . . . **5.20.7** CoaXPress CXP-12 – 12.500 Gbits/s
- **5.21 Avionics Digital Video Bus (ADVB)**
  - **5.21.1** ADVB At a Bit Rate of 1.0625 Gbit/s with 8B/10B encoding
  - **. . .**
  - **5.21.11** ADVB with 8B/10B encoding with 10.0000 Gbaud signaling

Summary

- **VITA, SOSA, HOST, and CMOSS communities giving input for revisions of OpenVPX standards**
- **ANSI/VITA 65.0-2021 and 65.1-2021 were published October 2021**
  - Added 16 of optical/coax Connector Modules
  - Added some protocols, only 1 new Slot Profile and 2 Backplane Profiles
  - Combinations enabled by optical/coax drove the addition of AMPS
- **With version of VITA 65.0 & 65.1, expected out early 2023**
  - Adding 2 Connector Modules with 75 ohm contacts to support video
  - Adding more protocol sections including sections for both analog and digital video
  - No new Slot or Backplane Profiles other than additional dash options
- **With version after 2023**
  - Expect new protocol sections, maybe some new Slot Profiles, Slot Profile dash options, …
- **There is ongoing work within VITA to develop a next generation VPX capability**



Backplane pictures courtesy of Elma